LMX9820ADEV: LMX9820A Simply Blue Module Kit User's Guide

National Semiconductor
User's Guide
December 2004
Revision 0.2

Scope

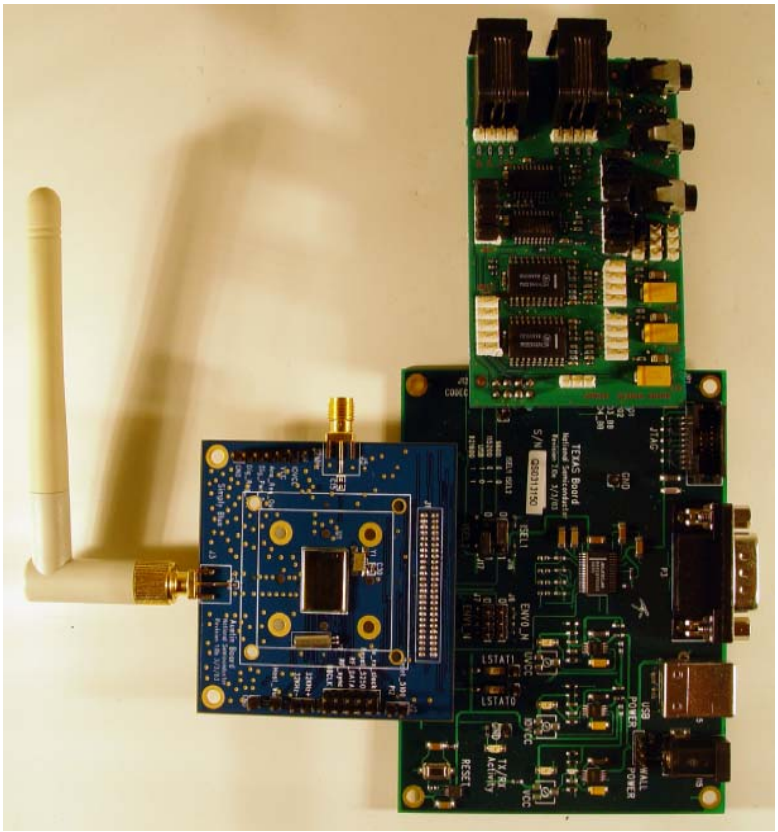
The Simply Blue module kit (LMX9820ADEV) is for evaluation and demonstration of the National Semiconductor® LMX9820A Simply Blue Serial Port module. This user's guide provides platform setup procedures and configuration options for the Simply Blue module kit.

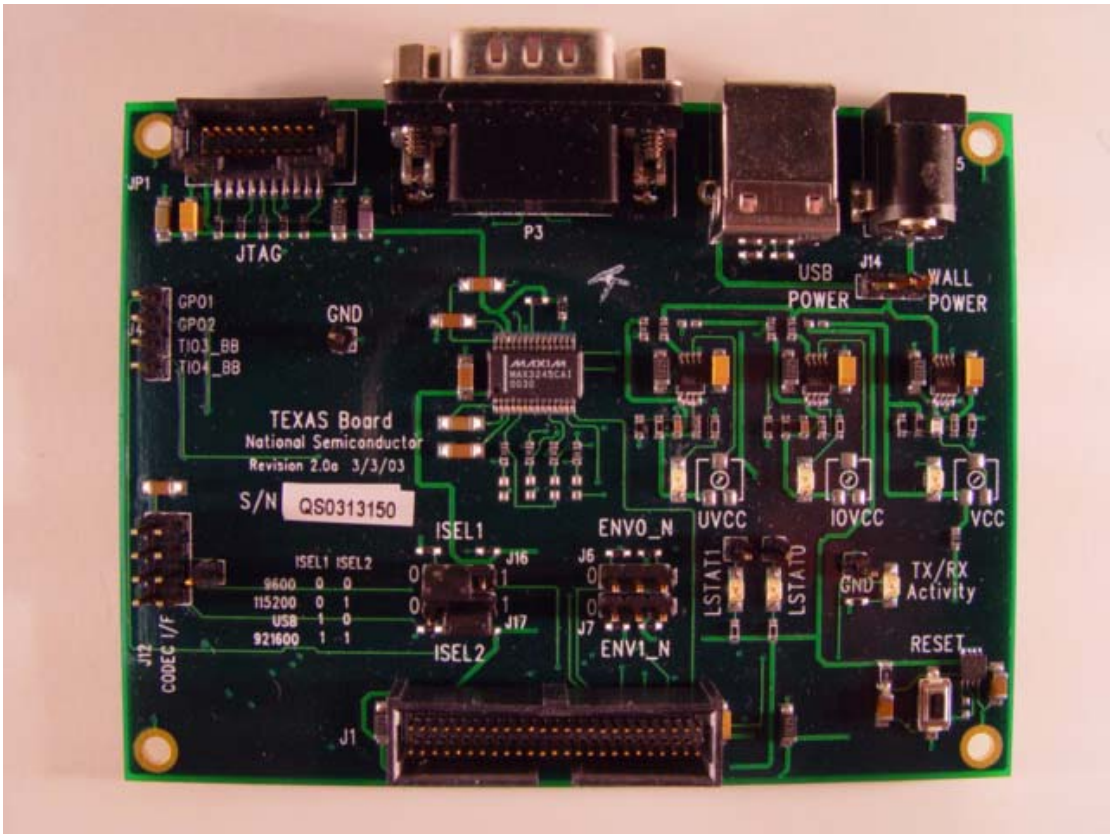
General Description

The Simply Blue module kit contains two boards:

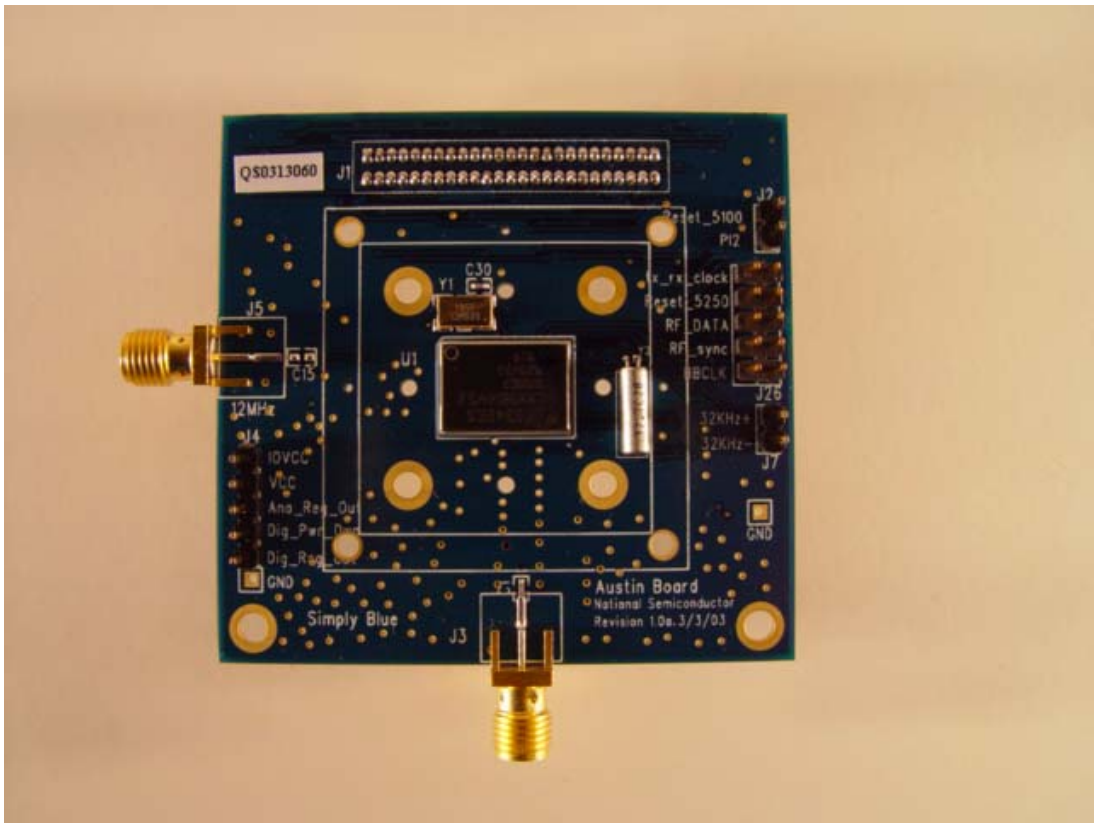
- Texas Motherboard Rev. 2
  - — Serial connector and RS-232 interface circuitry
  - — JTAG connector and interface circuitry
  - — Audio Codec interface for Sedona Board
  - — Three power regulators
  - — Power and link status LED indicators
  - — USB connector and interface circuitry (**not** used for LMX9820A)
  - — Test points of baseband and radio signals
  - — 50-pin connector (to Austin Daughterboard)
- Austin Daughterboard Rev. 1
  - — LMX9820A serial port module
  - — On-board 12 MHz crystal
  - — On-board 32.768 kHz crystal for low power modes
  - — Internal use only test points of module signals
  - — SMA connectors for antenna and clock
  - — 50-pin connector (to Texas motherboard)
- Sedona Audio Codec Daughterboard Rev. R1B
  - — 2 OKI Codecs, default operation
  - — 2 Motorola Codecs, supported
  - — 1 Speaker connection
  - — 2 Mic connections, only 1 used

LMX9820A Simply Blue Module Kit

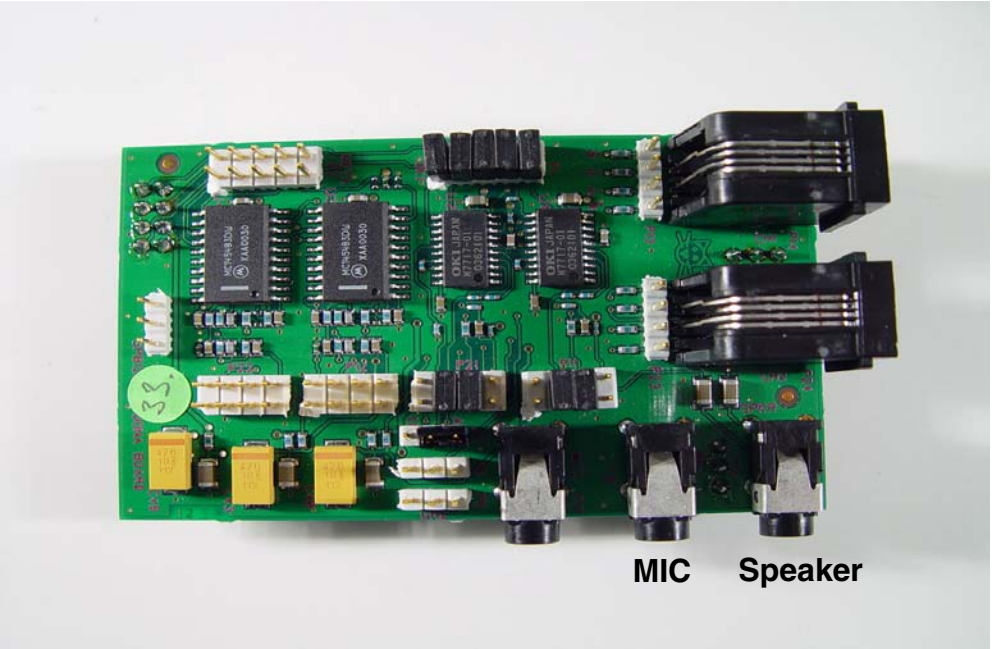




Texas Motherboard, Revision 2



Austin Daughterboard, Revision 1



Sedona Daughterboard, Revision 1

1.0 Kit Setup

1.1 KIT CONTENTS

The Simply Blue module kit (LMX9820ADEV) contains the following items:

- Texas Motherboard
- Austin Daughterboard
- Sedona Board
- Null modem cable
- 100V - 240V AC to 5V DC power supply
- Antenna
- CD-ROM containing documentation and software

1.2 REQUIREMENTS AND SETUP

1.2.1 Basic Requirements

- x86 PC with serial port
- One of the following Microsoft Windows Operating Systems is required:
  — Windows 2000
  — Windows XP

1.2.2 Software Included in Kit

- Simply Blue Commander:
  — Command oriented tool to generate commands and watch events on the Simply Blue Command interface
- CRISP In System Programmer (ISP)
  — Windows tool to update the on-chip firmware over the command interface
- SB Smart Demo Application
  — Windows tool for quick demo setup.

1.2.3 PC - Simply Blue Module Kit Setup

To set up the Simply Blue Commander:

1) Assemble the kit as shown in Figure 1-1.
2) Set ISEL1 and ISEL2 to UART at 115200 kbps or 921600 kbps, depending on the UART card in the PC. Reference Table 2-16 on page 9 for details on setting the UART interface.
3) Insert the kit CD. If the installation does not start automatically, double click *Setup.exe* on the root of the CD drive.
4) Click the *Install Software* button. Reference Figure 1-3 on page 5. This will install CRISP, documentation, SB Smart and Simply Blue Commander. Please browse the CD.
5) Shortcuts are installed at *Start->Programs->Simply Blue 2.0.* Reference Figure 1-4 on page 6.

For usage of the Simply Blue Commander refer to the "LMX982x Serial Port Module: Simply Blue Commander User's Guide"

1.2.4 CRISP In System Programmer (ISP) - Updating Firmware

Updating the firmware is possible by using the CRISP tool included on the CD-ROM. Kits are shipped with the current revision of firmware, so it is not necessary to update the kit immediately. Firmware updates will be released via the Wireless Developer's site or are available from local FAEs.

1) Assemble the kit as shown in Figure 1-1.
2) Launch CRISP from the installed short cuts. *Start->Programs->Simply Blue 2.0->CRISP*
3) Follow the CRISP User's Guide instructions. The guide must be followed closely.

If further assistance is required, contact your FAE or local National sales representative.

1.2.5 SB Smart

Reference the SB Smart User Guide.

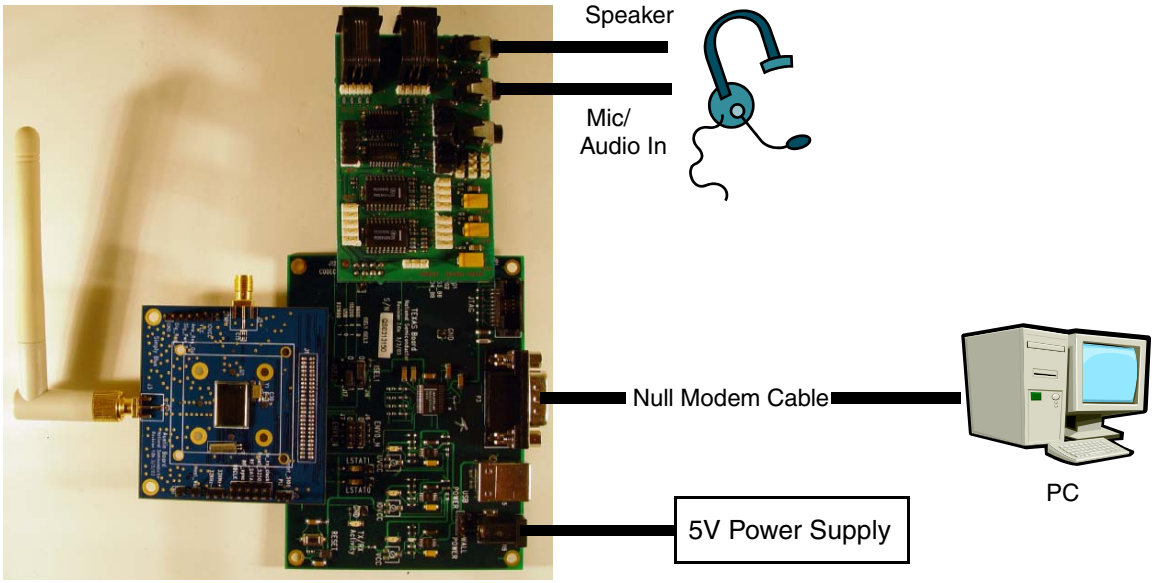


Figure 1-1. PC - Simply Blue Module Connection

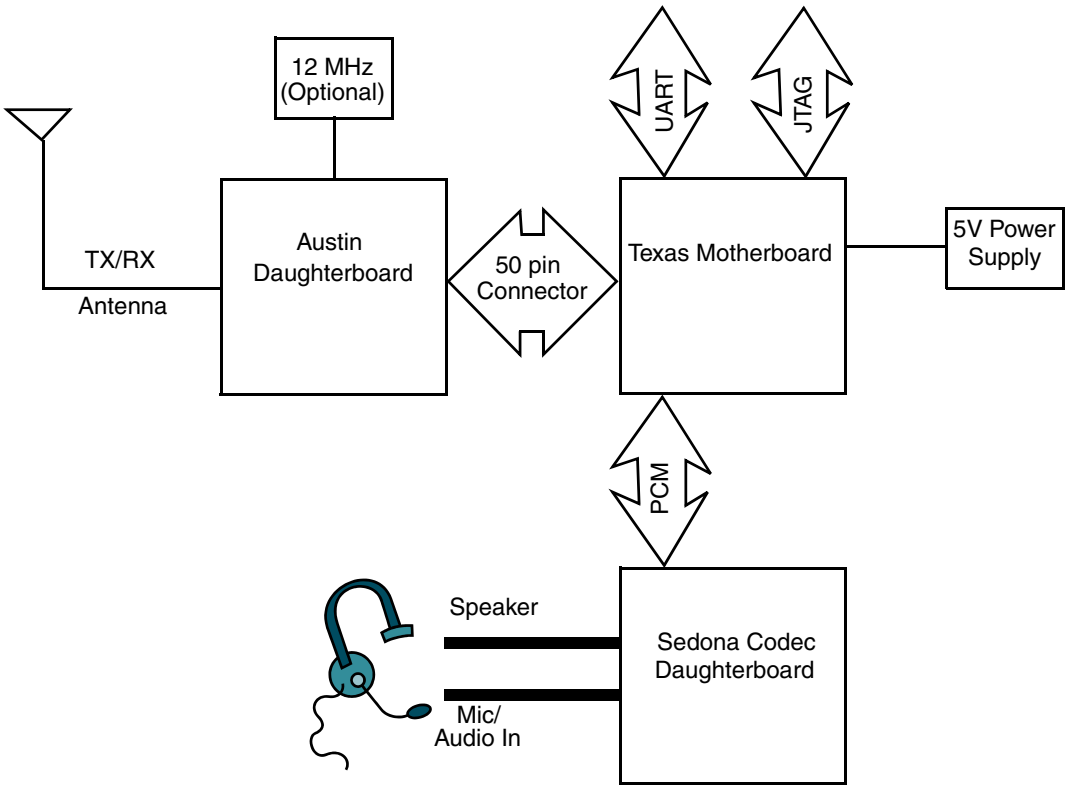


Figure 1-2. System Connection Diagram

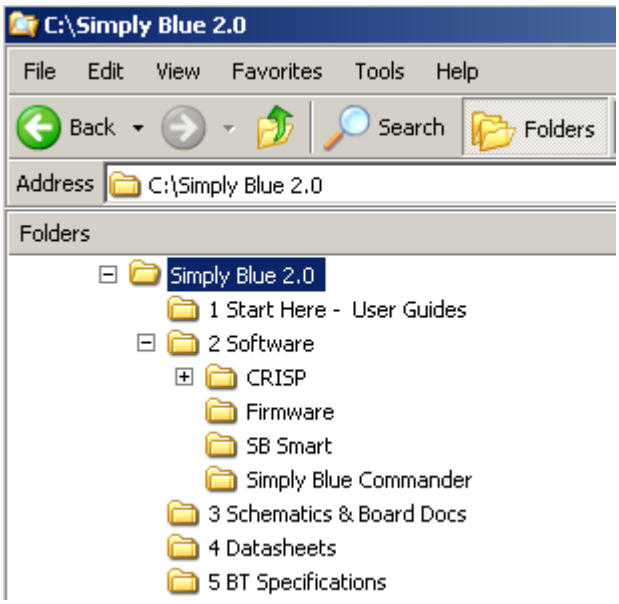


Figure 1-3. Simply Blue Default Directory

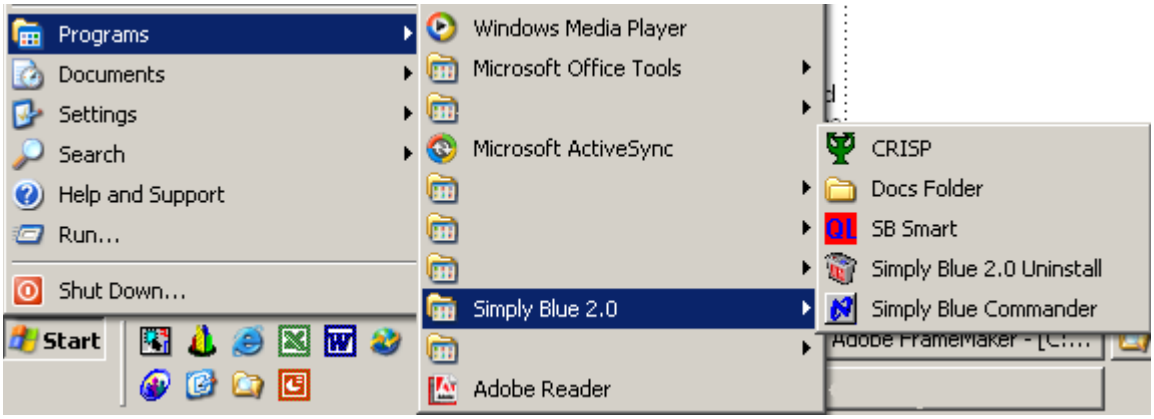


Figure 1-4. Simply Blue Shortcut

2.0 Board Components and Pin Assignments

A summary of the configuration and selection jumpers is provided in the tables that follow. Reference both the schematic and BOM (Bill of Materials) (included on the CD in the kit) and also available on the Wireless Developer's web site.

2.1 TEXAS MOTHERBOARD

- Table 2-1 lists the primary devices on the board.
- Table 2-2 lists the connectors, configuration, and selection jumpers.
- Table 2-3 lists the switches and LEDs.

Table 2-1. Texas Motherboard Primary Devices

Device #	Name
U2	National LP2986 Low-Dropout Voltage Regulator - IOVCC
U4	National LP2986 Low-Dropout Voltage Regulator - UVCC
U5	National LP2986 Low-Dropout Voltage Regulator - VCC
U46	Maxim MAX3245 1 Mbps High Speed UART Driver
U55	Toshiba TC7WH14FU Schmitt Inverter - Used for POR (Power On Reset) circuitry

Table 2-2. Connectors, Configuration, and Selection Jumpers Summary

Jumper #	Name	Details
P3	DP9 Serial Connector – Male	Table 2-4 on page 8
JP1	JTAG Connector (10x2)	Table 2-5 on page 8
J1	50-pin Connector to Austin Daughterboard	Table 2-23 on page 11
J4	Test Points and General Purpose Outputs	Table 2-6 on page 8
J5	USB (**not** used for LMX9820A)	Table 2-7 on page 8
J6	ENV0	Table 2-8 on page 8 and Table 2-10 on page 9
J7	ENV1	Table 2-9 on page 8 and Table 2-10 on page 9
J9/J22	GND	GND
J10	LSTAT_0	Internal Use Only
J11	LSTAT_1	Internal Use Only
J12	Audio Codec Header (4x2)	Table 2-12 on page 9
J14	USB or DC Power Supply Jumper	Table 2-13 on page 9
J15	DC Power Jack	Figure 2-2 on page 9
J16	ISEL1	Section 2.1.9 on page 9
J17	ISEL2	Section 2.1.9 on page 9
J23	Audio Codec Optional Test Point - User defined (**not** used for LMX9820A)	Table 2-12 on page 9

Table 2-3. Switches and LEDs

Name	Description
SW1	Reset# - Reset
D1	LED for LSTAT_0 (**not** used for LMX9820A)
D2	LED for LSTAT_1 - When illuminated, firmware has loaded properly
D3	LED for VCC
D4	LED for IOVCC
D5	LED for UVCC
D6	LED for TX/RX Activity

2.1.1 Schmitt Trigger for POR (Power On Reset)

A Schmitt Trigger for POR has been added to the Texas Motherboard to allow control of delay between VCC/IOVCC and RESET#. A minimum of 2 ms is required between VCC/IOVCC at rail and RESET# transition from low to high to have proper startup of the module.

2.1.2 P3 DP9 Serial Connector

P3 is a DP9 serial port connector that interfaces to the LMX9820A's full duplex UART. It supports up to 921.6 kbps transfer rates. Refer to Table 2-4 for selecting and setting the UART and transfer rate.

Table 2-4. P1 DP9 Pin Assignments

Pin #	Signal Name	Description
1	NC	No Connect
2	RDX	UART Receive Data input
3	TDX	UART Transmit Data output
4	NC	No Connect
5	GND	Ground
6	NC	No Connect
7	RTS#	UART Ready-To-Send output
8	CTS#	UART Clear-To-Send input
9	NC	No Connect

2.1.3 JP1 JTAG Connector

JP1 is a JTAG based serial on-chip debug interface. The JTAG interface allows the user fast program code download into the on-chip Flash program memory (e.g., firmware updates could be done via this interface).

Table 2-5. JP1 JTAG Connector Pin Assignments

Pin #	Signal Name	Description
1	RESET#	Reset - active low
2	IOVCC	IOVCC
3	NC	No Connect
4	GND	Ground
5	NC	No Connect
6	GND	Ground
7	TMS	JTAG Test Mode Select
8	GND	Ground
9	TDI	JTAG Test Data input
10	GND	Ground
11	TCK	JTAG Test Clock input
12	GND	Ground
13	TDO	JTAG Test Data output
14	GND	Ground
15	NC	No Connect
16	GND	Ground
17	NC	No Connect
18	GND	Ground
19	RDY#	JTAG Test Ready output - active low
20	NC	No Connect

2.1.4 J4 Test Points and General Purpose Output

J4 is a test point header and general purpose output connector. Test points are for internal use only and general purpose outputs are not currently utilized, not configured in firmware.

Table 2-6. J4 Pin Assignment

Pin #	Signal Name	Description
1	TIO4_BB	Test Point - internal use only
2	TIO3_BB	Test Point - internal use only
3	GPO2	General Purpose Output - not currently utilized
4	GPO1	General Purpose Output - not currently utilized

2.1.5 J5 USB Connector

Note: Not used for LMX9820A.

J5 is a USB (female), PCB mounting, 90° angled connector that interfaces with the USB transport layer in baseband. The on-chip USB module is compatible with USB specifications v1.0 and 1.1.

Table 2-7. J5 Pin Assignment

Pin #	Signal Name	Description
1	UVCC_5V	VCC USB
2	D-	USB D- upstream port
3	D+	USB D+ upstream port
4	GND	Ground USB

2.1.6 Mode Selection/ISP (In-System Programming) Configuration Header

Programming of the internal Flash can either be done over the JTAG interface or by starting a special ISP code, located in the boot area of the Flash. For normal Bluetooth operation, no jumpers are required on J6 or J7.

Table 2-8. J6 Pin Assignments

Pin #	Signal Name	Description
1	GND	Ground
2	ENV0	Refer to Table 2-10 for logic matrix
3	IOVCC	VCC

Table 2-9. J7 Pin Assignments

Pin #	Signal Name	Description
1	GND	Ground
2	ENV1	Refer to Table 2-10 for logic matrix
3	IOVCC	VCC

Table 2-10. Operation Environment [1]

ENV0 Input	ENV1 Input	Mode
0	1	ISP Firmware Upgrade
1	1	Normal Operation[2]

1. Refer to the LMX9820A datasheet for additional mode boot-up details.
2. A weak internal pull-up pulls ENV0/1 to VCC.

2.1.7 J12 Audio Header (4x2) and J23 Test Point

J12 provides access to the Advanced Audio Interface (AAI) signals that connect an external codec. The AAI is an advanced version of the SSI (Synchronous Serial Interface) that provides a full-duplex communications port to a variety of industry-standard 13-, 14-, 15-, and 16-bit linear or 8-bit log PCM codecs, DSPs, and other serial audio devices.

Table 2-11. J12 Pin Assignment

Pin #	Signal Name	Description
1	GND	Ground
2	SCK	AAI Clock
3	VCC	VCC
4	SFS	AAI Frame Synchronization
5	J23	Optional Test Point - user defined
6	STD	AAI Transmit Data output
7	GND	Ground
8	SRD	AAI Receive Data input

Table 2-12. J23 Pin Description

Pin #	Signal Name	Description
1	User Defined	J23 is user defined. Can be connected to one of the AAI signals for a test point or used for an external clock input.

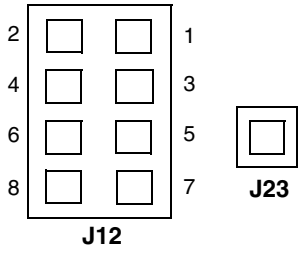


Figure 2-1. J12 and J23 Pin Identification

2.1.8 J14 USB or DC Power Supply

J14 selects between USB or DC (wall) power supply.

Table 2-13. J14 Jumper Pin Assignments

Pin #	Description
1-2	USB Power
2-3	DC (wall) Power Supply

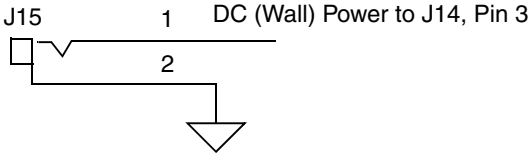


Figure 2-2. J15 DC Power Jack

2.1.9 J16 ISEL1 and J17 ISEL2 Interface Selection for UART and USB

Note: USB is **not** used for LMX9820A.

The interface selection pins ISEL1 and ISEL2 are used to provide different configurations after boot-up. See Table 2-14, Table 2-15, and Table 2-16 for the specific settings. The interface selection pin is used for transport layer selection. The USB interface is the standard 12 Mbps. The UART default baud rate is 921.6 kbps. If the UART is selected, the host controller must begin communications at 921.6 kbps. After communications are established, the host controller can then select baud rates between 38.4 kbps and 921.6 kbps via proprietary commands.

Table 2-14. J16 ISEL1 Pin Assignment

Pin #	Signal Name	Description
1	IOVCC	IOVCC
2	ISEL1	ISEL1
3	GND	Ground

Table 2-15. J17 ISEL2 Pin Assignment

Pin #	Signal Name	Description
1	IOVCC	IOVCC
2	ISEL2	ISEL2
3	GND	Ground

Table 2-16. J17 Pin Assignments[1]

ISEL1	ISEL2	Interface Speed (baud)	UART Settings
1	1	921.6	Check NVS
0	1	115.2	Check NVS
1	0	9.6 k	No parity, one stop bit
0	0	Check NVS	Check NVS

1. Default pins are internally set to 1 by weak pull-up.

2.2 AUSTIN DAUGHTERBOARD SUMMARY

The Austin Rev. 1 Daughterboard is populated with a 12 MHz crystal. Reference the schematic, BOM, and board for more details. Table 2-17 lists the primary devices on the board and Table 2-18 lists the connectors and headers.

Table 2-17. Austin Daughterboard Device Summary

Device #	Name
U1	National LMX9820A Serial Port Module - Reference the device datasheet.
Y1	12 MHz Crystal - Reference the crystal device datasheet and the LMX9820A datasheet for details.
Y2	32.768 kHz Crystal for low power modes - Reference the crystal device datasheet and the LMX9820A datasheet for more details.

Table 2-18. Connector and Header Summary

Connector/Header #	Name	Details
J1	50-pin Connector to Texas Motherboard	Table 2-23 on page 11
J2	2-pin Test Point	Table 2-19 on page 10
J3	SMA TX/RX Signal	Figure 2-3 on page 11
J4	5-pin Test Point	Table 2-20 on page 10
J5	SMA Optional External Clock	Figure 2-4 on page 11
J7	32.768 kHz 2-pin Test Point	Table 2-21 on page 10
J26	10-pin Test Point	Table 2-22 on page 10

2.2.1 J2 Test Point Header

J2 is a 2-pin test point header for internal use only.

Table 2-19. J2 Pin Assignments

Pin #	Signal Name	Description
1	Reset_5100	Reset to baseband - internal use only
2	P12	Test Point - internal use only

2.2.2 J4 Test Point Header

J4 is a 5-pin test point header for different voltage rails on the board.

Table 2-20. J4 Pin Assignments

Pin #	Signal Name	Description
1	IOVCC	Test point for IOVCC
2	VCC	Test point for VCC
3	VDD_ANA_OUT	Analog LDO output test point
4	VDD_DIG_PWR_D#	Digital LDO power down test point
5	VDD_DIG_OUT	Digital LDO power output test point

2.2.3 J7 Test Point Header

J7 is a 2-pin test point header for a 32.768 kHz crystal.

Table 2-21. J6 Pin Assignment

Pin #	Signal Name	Description
1	32.768 kHz +	32.768 kHz crystal
2	32.768 kHz -	32.768 kHz crystal

2.2.4 J26 Test Point Header

J26 is a 10-pin test point header for the CCB interface, TR Switch, Reset#, and BBCLK. These are provided for debug purposes.

Table 2-22. J26 Pin Assignment

Pin #	Signal Name	Description
1	GND	Ground
2	BBCLK	12 Mhz Baseband Clock Test Point
3	CCB_LATCH	Serial Data Latch Test Point
4	TX_RX_SYNC	Test Point - internal use only
5	SDAT	Serial Data Test Point
6	RF_DATA	Test Point - internal use only
7	CCB_CLOCK	Serial Data Clock Test Point
8	RESET#	Reset - active low
9	TR_SWITCH	TR Switch Test Point
10	TX_RX_CLOCK	Test Point - internal use only

2.2.5 J3 SMA RF Signal Connector

Connect antenna or test equipment to the SMA.

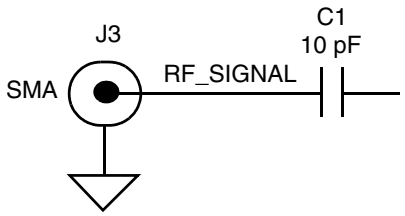


Figure 2-3. J3 SMA Connection - Single TX/RX

2.2.6 J5 Optional External Clock

An optional external clock can be used. C29, 100 pF, must be placed for proper operation. It is recommended to set the signal generator to 12 MHz @ 2 dBm output. Refer to Figure 2-4.

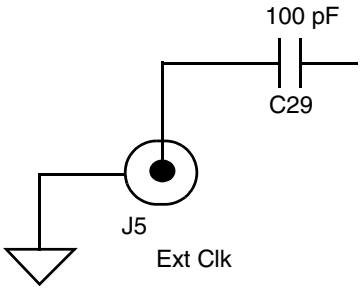


Figure 2-4. J5 SMA Connection - (Optional) External Clock Input

2.2.7 J1 Connector

J1 is a 50-pin board-to-board connector. See Table 2-23 for pin assignments.

Table 2-23. J1 Pin Assignments

Pin #	Signal Name	Description
1	TMS	JTAG - Test Mode Select input
2	D+	USB DATA+
3	TDI	JTAG - Test Data input
4	D-	USB DATA-
5	TDO	JTAG - Test Data output
6	UVCC	UVCC
7	TCK	JTAG - Test Clock input
8	GND	Ground
9	RDY#	JTAG - Ready output (active low)
10	VCC	VCC
11	GND	Ground
12	GND	Ground
13	SCK	AAI - Clock
14	IOVCC	IOVCC
15	SFS	AAI - Frame Synchronization
16	GND	Ground

Table 2-23. J1 Pin Assignments (Continued)

Pin #	Signal Name	Description
17	STD	AAI - Transmit Data output
18	NC	No Connect
19	SRD	AAI - Receive Data input
20	NC	No Connect
21	GND	Ground
22	GND	Ground
23	RESET#	Reset for LMX5100
24	NC	No Connect
25	LSTAT_0	Link Status Bit 0 output
26	GND	Ground
27	LSTAT_1	Link Status Bit 1 output
28	NC	No Connect
29	ENV0	Module Operating Environment Input Bit 0
30	GND	Ground
31	ENV1	Module Operating Environment Input Bit 1
32	TIO3_BB	Internal use only
33	SDAT	Serial Data
34	GND	Ground
35	GND	Ground
36	RDX	UART Receive Data input
37	ISEL2	Interface Select 2
38	TDX	UART Transport - Transmit Data
39	ISEL1	Interface Select 1
40	CTS#	UART Transport - Clear-to-Send
41	TIO4_BB	Internal use only
42	RTS#	UART Transport - Request-to-Send
43	GPIO1_RF	Internal use only
44	GND	Ground
45	GPIO2_RF	Internal use only
46	RFDATA	RF Antenna Port - 50Ω nominal impedance
47	GND	Ground
48	GND	Ground
49	GND	Ground
50	TR Switch	TR Switch

2.3 SEDONA CODEC DAUGHTERBOARD SUMMARY

The Sedona codec Rev. R1B Daughterboard is populated with a 2 OKI codecs and 2 Motorola codes. Oki codec is the only supported device. Also, no configuration is needed for board so full details are not provided. Reference the schematic, BOM, and board for more details. Table 2-24 lists the primary devices on the board

Table 2-24. Sedona Codec Daughterboard Device Summary

Device #	Name
U1, U2	Oki codec MSM7717
U3, U4	Motorola codec MC145483

Table 2-25. Connector and Header Summary

Connector/Header #	Name	Details
P3	Connector to Texas Board	Table 2-26 on page 12
Speaker Jack	Connector for speaker or headset	Figure 2-5 on page 12
Microphone Jack	Connector for microphone	Figure 2-6 on page 12

2.3.1 P3 Connector to Texas Board

P3 is a 8-pin connector to connect to the Texas board codec interface.

Table 2-26. P3 Pin Assignments

Pin #	Signal Name	Description
1	SCK	AAI Clock
2	GND	Ground
3	SFS	AAI Frame Synchronization
4	VCC	VCC
5	STD	AAI Transmit Data output
6	SFS1	Not used since only single channel used
7	SRD	AAI Receive Data input
8	GND	Ground

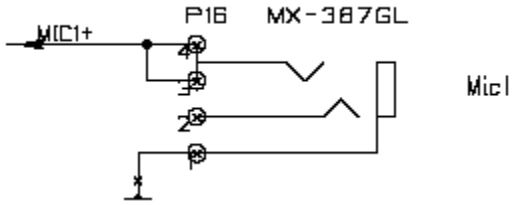


Figure 2-6. Microphone Jack

2.3.2 Speaker Jack

Connect to headset or speaker.

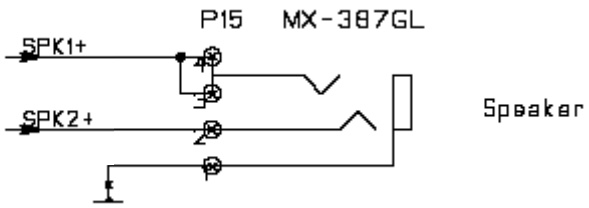


Figure 2-5. Speaker Jack

2.3.3 Microphone Jack

Connect to microphone.

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